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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,259	LIPPINCOTT, LOUIS A.	
	Examiner	Art Unit	
	Dalip K. Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *8,16,20,22 and 26-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-15,17-19,21 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated January 4, 2005 in response to PTO Office Action dated June 29, 2004. The amendments to claim(s) 1, 4, 5, 9, 15, 17, 18, 21, 23 and 24; and the cancellation of claim(s) 8, 16, 20, 22 and 26-30 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below. The applicant's amendment errenously states claim 26 being amended wherein it has been actually cancelled.

2. With respect to applicant's argument for claim 1 that, "Yoshiba teaches away from an entire region being copied and that only the data in the desired part 420 may be read out of the VRAM 16", Fig. 14 clearly shows a entire region 420 of VRAM#1 b being copied and transferred to the CRT 10. Yoshiba does not explicitly discloses plurality of regions similarly as per instant claim 1 limitation but copying of a region of VRAM#1 is similar to copying of a region data for displaying on the CRT. For the sake of argument, Yoshiba being not explicit about buffer being divided into a plurality of regions, Callahan et al. **discloses** an offscreen buffer and an onscreen buffer wherein these buffers are tiled for efficient memory operations (...in one implementation,...onscreen buffered graphics are tiled...in another implementation, off-screen buffered graphics are tiled also....col. 2, lines 40-67; col. 3, lines 1-15) from which copying of the entire region (tile) takes place.

3. Applicant's arguments filed January 4, 2005 have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 3, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Reference 4,816,815 to Yoshiba in view of U.S. Patent No. 6,396,473 to Callahan et al.

a. Regarding claim 1, Yoshiba **discloses** a dual frame buffer system (Figure 1), comprising: a first frame buffer (first display memory (VRAM) 16); a second frame buffer (second VRAM 24); and a controller (CRTC 22) for copying updated data from the first frame buffer (first display memory (VRAM) 16) to the second frame buffer (second VRAM 24) when updated data is needed to refresh the display monitor (col. 3, lines 47-68; col. 4, lines 1-8). Yoshiba **is silent about** a first frame buffer being divided into a plurality of regions. Callahan et al. **discloses** an offscreen buffer and an onscreen buffer wherein these buffers are tiled for efficient memory operations (...in one implementation,...onscreen buffered graphics are tiled...in another implementation, off-screen buffered graphics are tiled also....col. 2, lines 40-67; col. 3, lines 1-15) and employs two techniques for dynamic updating/copying of data from offscreen/onscreen buffers (tiles). Firstly, in case of insufficient memory space for indirect and invisible processing, the offscreen graphic buffer is processed directly to the existing onscreen tiles within the onscreen buffer (...two techniques may be used to update tiles within the onscreen buffer...new tiles are created and swapped in...the tiles created so far are swapped into the onscreen buffer...until the update is complete...col. 10, lines 9-46). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Yoshiba with the feature "tiled regions of frame buffers which are copied to the display as they are updated" as taught by Callahan et al. **because** it results in significant memory savings (col. 12, lines 7-20).

b. Regarding claim 2, Yoshiba et al. **discloses** wherein the controller (CRTC 22) coordinates refresh of the display monitor using data stored in the second frame buffer (second VRAM 24) and data updated within the first frame buffer (first display memory (VRAM) 16) (col. 4, lines 3-5).

c. Regarding claims 3 and 11, Yoshiba **discloses** the dual frame buffer system, further comprising: a first address generator (display address counter 155, Fig. 5) corresponding to the first frame buffer (display data buffer 164, Fig. 5); a second address generator (display address counter 130, Fig. 5) corresponding to the second frame buffer (display data buffer 166); and a timing generator (sync signal generator for crt 158) for coordinating the timing between the first and second address generators (display address counter 155, 130 Fig. 5) for refreshing the display monitor.

d. Regarding claims 10, it is similar in scope to claim 2 above and is rejected under the same rationale.

6. Claims 4-6, 12-15, 17-19, 21, 23, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,816,815 to Yoshiba in view of U.S. Patent No. 6,396,473 to Callahan et al as applied to claim 1 above, and further in view of U.S. Patent No. 5,757,364 to Ozawa et al.

a. Regarding claims 4 and 12, Yoshiba-Callahan combination **does not disclose** a detector for detecting when an update is made to the data in the first frame buffer; and a decoder for decoding the location of the updated data. Ozawa et al. **discloses** a detector (window type table 132, comparator 118) for detecting when an update is made to the data in the first frame buffer; and a decoder (selector 121) for decoding the location of the updated data (col. 4, lines 36-48; col. 5, lines 1-67; col. 6, lines 1-41). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was

made to modify Yoshiba-Callahan with the feature "detector and decoding and transmitting only the updated data" as taught by Ozawa et al. **because** it provides for efficiently rendering frames by transmitting only the updated data and provides for efficient real time displaying dynamic images (col. 1, lines 40-67).

b. Regarding claims 5 and 13, Yoshiba as modified by Callahan et al. **discloses** wherein the first frame buffer comprises a plurality of regions (...in one implementation,...onscreen buffered graphics are tiled...in another implementation, off-screen buffered graphics are tiled also....col. 2, lines 40-67; col. 3, lines 1-15) ...two techniques may be used to update tiles within the onscreen buffer...new tiles are created and swapped in...the tiles created so far are swapped into the onscreen buffer...until the update is complete...col. 10, lines 9-46). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Yoshiba with the feature "tiled regions of frame buffers which are copied to the display as they are updated" as taught by Callahan et al. **because** it results in significant memory savings (col. 12, lines 7-20) (col. 3, lines 56-65).

c. Regarding claims 6 and 14, they are similar in scope to claim 4 above and are rejected under the same rationale.

d. Regarding claims 15, 17, 21 and 23, they are similar in scope to claim 12 above and are rejected under the same rationale.

e. Regarding claims 18 and 24, they are similar in scope to claim 13 above and are rejected under the same rationale.

f. Regarding claims 19 and 25, they are similar in scope to claim 14 above and are rejected under the same rationale.

7. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,816,815 to Yoshiba in view of U.S. Patent No. 6,396,473 to Callahan et al as applied to claim 1 above, and further in view of U.S. Patent No. 5,790,138 to Hsu.

a. Regarding claims 7 and 9, Yoshiba-Callahan combination **does not disclose** wherein the first frame buffer is part of a unified memory architecture. Hsu **discloses** a computer unified memory architecture system wherein the first frame buffer (frame buffer memory 304b) is part of a unified memory architecture (col. 3, lines 65-67; col. 4, lines 1-9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Yoshiba-Callahan with the feature "frame buffer as part of a unified memory architecture" as taught by Hsu **because** it provides for a lower system cost (col. 1, lines 62-65).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(571) 272-7778**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dalip K. Singh
Examiner , Art Unit 2676

dks
June 2, 2005

Kee M. Tung
Primary Examiner